The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

a first step of forming an insulating film on a semiconductor layer;

a second step of forming a conductive layer on the insulating film;

a third step of selectively etching the conductive layer, forming a conductive layer having a first tapered shape;

a fourth step of doping a single conductivity type impurity element into the semiconductor layer, after completing the third step;

a fifth step of selectively etching the conductive layer having the first tapered shape, forming a conductive layer having a second tapered shape; and

a sixth step of doping a single conductivity type impurity element into the semiconductor layer overlapped with the second tapered shape, after completing the fifth step,

wherein the concentration of the single conductivity type impurity element doped in the sixth step is lower than the concentration of the single conductivity type impurity element doped in the fourth step.

2. (Currently Amended) A method of manufacturing a semiconductor device having an n-channel thin film transistor, comprising:

a first step of forming an insulating film on a semiconductor layer which forms the n-channel thin film transistor;

a second step of forming a conductive layer on the insulating film;

a third step of selectively etching the conductive layer, forming a conductive layer having a first tapered shape;

a fourth step of doping a single conductivity type impurity element into the semiconductor layer, after completing the third step;

a fifth step of selectively etching the conductive layer having the first tapered shape, forming a conductive layer having a second tapered shape; and

a sixth step of doping a single conductivity type impurity element into the semiconductor layer overlapped with the second tapered shape, after completing the fifth step,

wherein the concentration of the single conductivity type impurity element doped in the sixth step is lower than the concentration of the single conductivity type impurity element doped in the fourth step.

3. (Currently Amended) A method of manufacturing a semiconductor device having an n-channel thin film transistor and a p-channel thin film transistor, comprising:

a first step of forming an insulating film on a semiconductor layer of the n-channel thin film transistor and on a semiconductor layer of the p-channel thin film transistor;

a second step of forming a conductive layer on the insulating film;

a third step of selectively etching the conductive layer, forming a conductive layer having a first tapered shape;

a fourth step of doping a single conductivity type impurity element into the semiconductor layers, after completing the third step;

a fifth step of selectively etching the conductive layer having the first tapered shape, forming a conductive layer having a second tapered shape;

a sixth step of doping a single conductivity type impurity element into the semiconductor layers overlapped with the second tapered shape, after completing the fifth step, and

a seventh step for doping an impurity element, having a conductivity type which is inverse to the conductivity type of the single conductivity type impurity element, into the semiconductor layer of the p-channel thin film transistor, after completing the sixth step;

wherein the concentration of the single conductivity type impurity element doped in the sixth step is lower than the concentration of the single conductivity type impurity element doped in the fourth step.

4. (Currently Amended) A method of manufacturing a semiconductor device having a pixel portion, comprising:

a first step of forming an insulating film on a semiconductor layer that forms a thin film transistor provided in each pixel of the pixel portion;

a second step of forming a conductive layer on the insulating film;

a third step of selectively etching the conductive layer, forming a conductive layer having a first tapered shape;

a fourth step of doping a single conductivity type impurity element into the semiconductor layer, after completing the third step;

a fifth step of selectively etching the conductive layer having the first tapered shape, forming a conductive layer having a second tapered shape; and

a sixth step of doping a single conductivity type impurity element into the semiconductor layer overlapped with the second tapered shape, after completing the fifth step,

wherein the concentration of the single conductivity type impurity element doped in the sixth step is lower than the concentration of the single conductivity type impurity element doped in the fourth step.

5. (Original) The method of manufacturing a semiconductor device according to claim 1, wherein the angle of the tapered portion of the gate electrode having the tapered portion is greater than or equal to 30° and less than or equal to 60°.

6. (Original) The method of manufacturing a semiconductor device according to claim 1, wherein the gate electrode having the tapered portion is composed of an element selected from the group consisting of tungsten, tantalum, and titanium, or a compound of said elements, or an alloy of said elements.

7. (Original) The method of manufacturing a semiconductor device according to claim 2, wherein the angle of the tapered portion of the gate electrode having the tapered portion is greater than or equal to 30° and less than or equal to 60°.

8. (Original) The method of manufacturing a semiconductor device according to claim 3, wherein the angle of the tapered portion of the gate electrode having the tapered portion is greater than or equal to 30° and less than or equal to 60°.

9. (Original) The method of manufacturing a semiconductor device according to claim 4, wherein the angle of the tapered portion of the gate electrode having the tapered portion is greater than or equal to 30° and less than or equal to 60°.

10. (Original) The method of manufacturing a semiconductor device according to claim 2, wherein the gate electrode having the tapered portion is composed of an element selected from the group consisting of tungsten, tantalum, and titanium, or a compound of said elements, or an alloy of said elements.

11. (Original) The method of manufacturing a semiconductor device according to claim 3, wherein the gate electrode having the tapered portion is composed of an element selected from the group consisting of tungsten, tantalum, and titanium, or a compound of said elements, or an alloy of said elements.

12. (Original) The method of manufacturing a semiconductor device according to claim 4, wherein the gate electrode having the tapered portion is composed of an element selected from the group consisting of tungsten, tantalum, and titanium, or a compound of said elements, or an alloy of said elements.

13. (Original) The method of manufacturing a semiconductor device according to claim 5, wherein the gate electrode having the tapered portion is composed of an element selected from the group consisting of tungsten, tantalum, and titanium, or a compound of said elements, or an alloy of said elements.